The IRIDIUM® K-Band MMIC Chip Set

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Abstract: A set of 16 K-band MMIC chips has been developed for the satellites in the IRIDIUM® communications program[1]. Both high power and low noise 0.25 μm PHEMT technologies were used to develop this MMIC chip set. The MMICs consist of a broad band frequency doubler, up and down converters, high power amplifiers, variable gain amplifiers, low noise amplifiers, and an IF amplifier. A noise figure of less than 3.3 dB at 29 GHz and output power of over 4 watts at 23.3 GHz were achieved with no RF tuning. This paper describes statistical device characterization, design details, measured results, and integration of these MMIC chips into a high density multi-chip module (MCM).

Introduction

The high volume and aggressive schedule associated with the production of satellites in the IRIDIUM® communications program[1] demanded that two highly producible and reliable K-band T/R converter modules be developed. To achieve these goals, MMIC technology was used. Sixteen custom K-band MMICs were developed using 0.25 μm GaAs PHEMT technology. Eleven of these chips were developed for a low noise MMIC process and five were developed for a double gate recess power MMIC process. This paper discusses the design approach, application, and test results of this MMIC chip set.

Low Noise MMICs

Two separate K-band up and down converter chains were developed on the MiSig 0.25 μm low noise GaAs PHEMT process. The ground to satellite link was developed at a uplink frequency of 29.2 GHz and a downlink frequency of 19.5 GHz. The satellite to satellite link was designed to transmit and receive at a frequency of 23.3 GHz. Each link had an IF frequency of 750 MHz.

Two LNA MMICs were designed with greater than 12 dB of gain to establish the front-end noise figure of less than 3.4 dB at 23.3 GHz and 29.2 GHz. The 23.3 GHz LNA includes an input blanking switch to protect the LNA from high power reflections off the antenna during transmit mode.

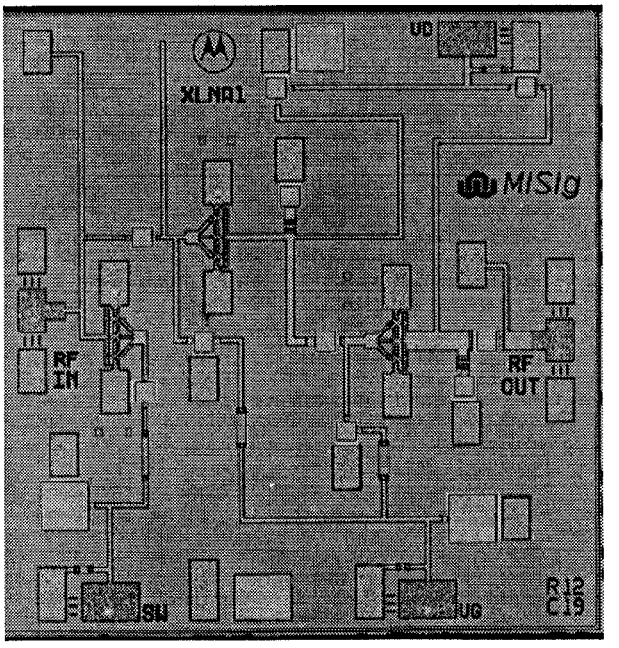

Figure 1: 23.3 GHz Low Noise Amplifier

The converter MMIC chips developed contain an IF and LO amplifier and a single balanced mixer. The up converters contain an additional RF amplifier. The down and up converter chips were designed with a conversion gain of 3 dB and 13 dB respectively. A separate IF amplifier chip was developed to provide additional gain.

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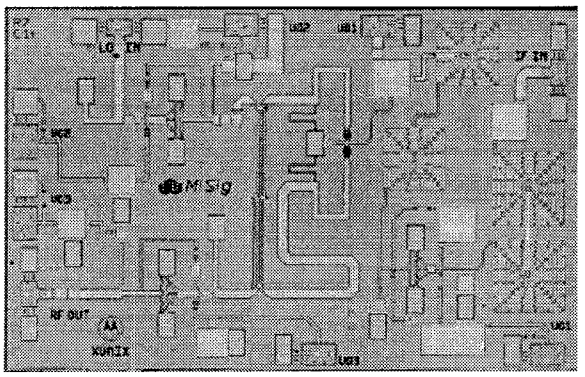

Figure 2: 0.75 to 23.3 GHz Up Converter

A broad band doubler MMIC chip was developed with a minimum 16 dB conversion gain and 20 dB fundamental rejection over the output frequency band of 16 to 32 GHz.

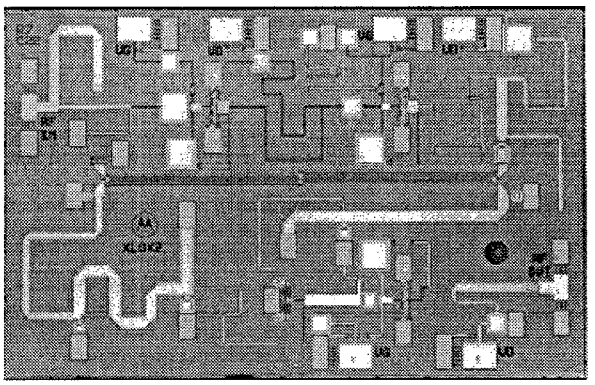

Figure 3: 16 to 32 GHz Doubler

Two 3-stage low noise VGAs were developed for the 23.3 and 29.2 GHz down converters. A single 2-stage wide band VGA was designed to cover both 19.5 and 23.3 GHz up convert bands. The VGAs were designed to have a gain adjustment range of 6 to 8 dB which was used for gain compensation over temperature. Gain control was accomplished by varying the FET drain current.

High Power MMIC Chips

Two separate K-band power amplifier chains were designed, one at 23.3 GHz which delivered over 4 watts, and one at 19.5 GHz which delivered 0.8 watts. Both amplifiers were developed with greater than 40 dB gain and high linearity to meet spectral regrowth and AM/PM conversion requirements.

At 19.5 GHz, a 2-stage high power MMIC amplifier was designed to provide 29.2 dBm of output power at 1 dB compression with an associated gain of over 15 dB.

Another high power MMIC amplifier with 13 dB gain and a P1dB of 31 dBm was developed to achieve a 4-way combined output power of 4 Watts at 23.3 GHz. The 4-way output combiner was designed using a suspended substrate combiner for lower loss.

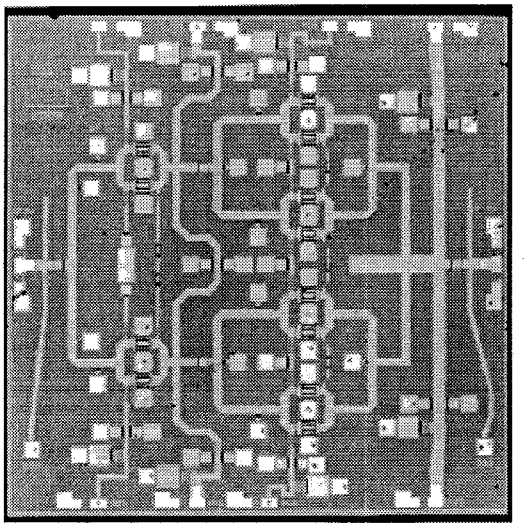

Figure 4: 19.5 GHz High Power Amplifier

The high power amplifier MMICs were driven by 2-stage medium power amplifier chips. Finally, a wide band MMIC amplifier was designed to provide an additional 17 dB of gain for both power amplifier chains.

Statistical Device Characterization

In order to minimize the effect of process variability on electrical performance, a statistical design methodology was developed. The methodology started with direct extraction[1] of noise parameters, small-signal models, and large-signal models in a statistically sampled fashion.

Statistical models were developed for the MiSig 0.25x150 μm low noise PHEMT pi-gate FET and 60 μm diode. FET models were developed at 3 different bias points for optimal noise figure and gain performance. Both FET and diode models were verified using 0.045 to 40 GHz measured s-parameters and 2 to 26 GHz measured noise parameters. A modified Fukui noise model[2] was derived using the statistical small signal model parameters and measured noise parameters, resulting in correlated small signal and noise model parameters. This model was successfully used to extrapolate beyond the 2-26 GHz measured noise parameters with excellent correlation (see Figure 6).

Statistical models were also derived for the Raytheon 600 μm and 1200 μm interdigital double gate recess power PHEMTs. Measured s-parameters were obtained

at 25 bias points across the I-V plane. Bias points along the projected operating load line were emphasized to increase the accuracy of the large signal model as shown in Figure 5. Custom software[3] was then used to extract

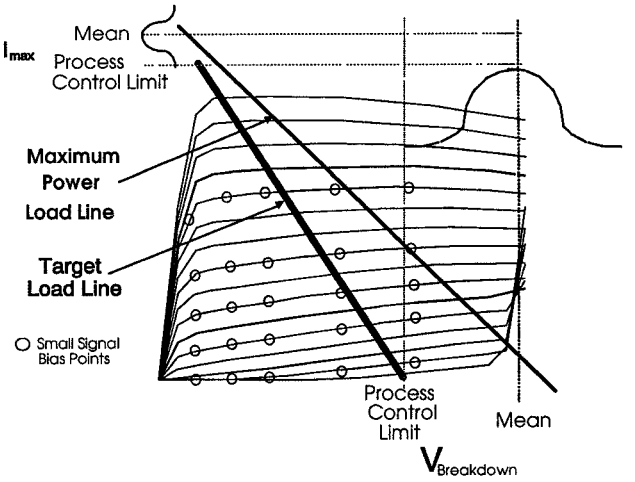

Figure 5: Load Line and Bias Points for Model Extraction

an Advanced Curtice large signal model which best fit the multiple bias small signal data. The final large signal models were revalidated at various points along the load line by comparing large signal calculated and measured s-parameters. Load-pull measurements were also made to further verify model accuracy.

MMIC Design

Breaking from the traditional worst case approach, each specification was statistically allocated from the system level in terms of mean and standard deviation. Yield optimization was done through a set of Design of Experiments (DOE). A simulated experiment was done to evaluate initial circuit performance variation and determine which factors had a significant effect on performance. The variables used in the DOE included both active device model parameters and matching elements. A second set of simulated experiments was done to determine any interaction effects between the significant factors and matching elements in the design. These interaction effects were used advantageously to minimize variations in overall circuit performance. A final set of simulations was done to estimate the mean and standard deviation of the design.

Power amplifier device load lines were set to maximize yield rather than output power. Figure 5 illustrates the target load line that was tolerant to expected MMIC process variations. This approach provided consistent RF power performance regardless of variation in MMIC fabrication. Device peripheries were then sized to meet output power requirements with the high yield load line. All power amplifiers were biased Class AB as a compromise between device efficiency and linearity. Class B and C operation proved impractical due to their low associated gain levels. Class AB operation also had the advantage over class A of reducing DC power consumption at low RF drive levels.

Stability was a major concern due to the high gain of PHEMT devices. Therefore, the drains of all low noise devices and the gates of all active power device unit cells were resistively loaded to provide unconditional stability to greater than 40 GHz. Low source inductance was found to improve device gain and high frequency stability, therefore, active device cells were limited to 600 μm periphery. This was accomplished by inserting source vias between the 600 μm cells to break up large periphery devices and then power combining the device cells. Differential resistors were also employed between device drain pads to suppress odd-mode oscillations in the power amplifiers. In addition, all possible feedback paths were analyzed to prevent loop oscillations.

The chip set was designed with 50 ohm port impedances to accommodate chip level testing. Interconnection of MMICs was accomplished using a wire bond interface developed on the program. The interface is used to present a wide band 50 ohm impedance to the MMICs resulting in identical in-circuit and chip level probed test data.

Low Noise MMIC Performance

A statistical sample of each chip design was measured and compared with the allocated specifications. Table 1 shows the low noise chip set results.

Chip Name	Freq. (GHz)	Gain μ (dB)	Gain σ (dB)	NF μ (dB)	NF σ (dB)
XLNA	22-24	18.9	1.2	2.7	0.1
XVGA	22-24	22.96	1.45	4.51	0.36
GLNA	29-30	15.34	.52	2.9	0.37
GVGA	29-30	22.8	1.2	4.3	0.3
VGAUP	19-24	17.9	1.15	N/A	N/A
XDMIX	22-24	2.83	1.1	N/A	N/A
GDMIX	29-30	3.4	1.25	N/A	N/A
XUMIX	22-24	11.8	0.9	N/A	N/A
GUMIX	29-30	12.1	1.6	N/A	N/A
LOX2	16-32 out	16.35	1.5	N/A	N/A
IFAMP	0.6-0.9	9.7	.53	N/A	N/A

Table 1: Low Noise MMIC Performance

Based on the results, the design methodology used proved to be beneficial in producing MMIC chips with high RF yields. All input and output return losses, with the exception of the input return loss of the LNAs, were better than 12 dB, to prevent mismatch loss and ripple.

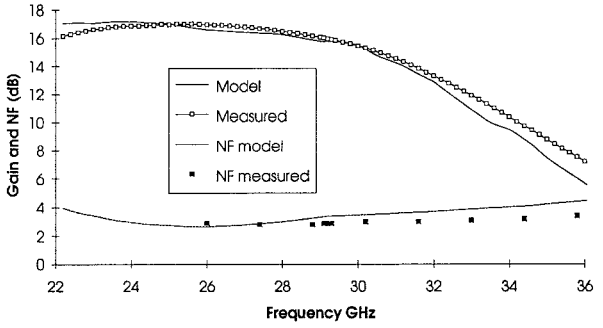

Figure 6: 29.2 GHz LNA Performance

Power Amplifier Performance

The performance of the five power MMIC chips is summarized in Table 2.

Chip Name	Freq GHz	Output Gate Width mm	Gain μ dB	Gain σ dB	P_{1dB} μ dBm	P_{1dB} σ dBm
XTHPA	23.3	4.0	13.5	1.1	30.7	0.7
XTMPA	23.3	2.4	14.4	0.5	25.8	0.5
PAIN	19-24	0.2	17.4	0.3	15.1	0.5
GTHPA	19.5	3.2	15.2	0.9	29.2	0.7
GTMPA	19.5	1.2	16.1	0.9	25.4	0.5

Table 2: MMIC Chip Performance

Figure 7 shows the measured gain performance of the 19.5 GHz high power amplifier along with predicted 3 standard deviation performance limits.

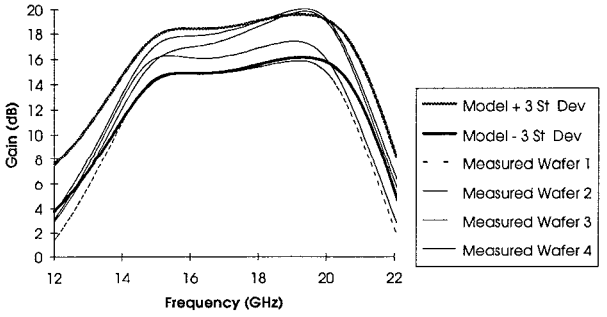

Figure 7: High Power Amplifier MMIC Performance

Integrating these chips into the power amplifier chains, a measured gain of 59.5 dB and P1dB of 29.2 dBm was achieved at 19.5 GHz and a gain of 49.2 dB and P1dB of 36.4 dBm was achieved at 23.3 GHz.

Because of the accuracy of the statistical models and the high performance of the wire bond interfaces, both of the integrated power amplifiers performed virtually identical to the statistical model predictions with no RF tuning required.

Summary

Sixteen custom K-band 0.25 μm PHEMT MMICs have been developed for the satellites in the IRIDIUM® communication program[2]. Statistical models were extracted and their utility to the high frequency design domain demonstrated. Since high producibility was an important design goal, MMIC RF yield rather than maximum performance was emphasized. The design goal of no RF tuning in these two K-band multi-chip modules was met.

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